**Basic Design Rule Check (DRC) in Cadence Allegro**

1. **What is the main purpose of running a Design Rule Check (DRC) in Cadence Allegro?**
   * a) To generate the netlist for the design
   * b) To check that the design follows all predefined physical and electrical rules
   * c) To create the Bill of Materials (BOM)
   * d) To simulate the electrical performance of the circuit

**Answer:** b) To check that the design follows all predefined physical and electrical rules

1. **Which of the following can be checked during a DRC in Cadence Allegro?**
   * a) Trace width violations
   * b) Clearance between components
   * c) Unconnected pins
   * d) All of the above

**Answer:** d) All of the above

1. **What does DRC stand for in Cadence Allegro?**
   * a) Design Rule Check
   * b) Design Resource Control
   * c) Device Reliability Check
   * d) Design Rating Control

**Answer:** a) Design Rule Check

1. **When should you perform a DRC in Cadence Allegro?**
   * a) After schematic capture
   * b) After completing the PCB layout design
   * c) Before and after applying constraints in the design
   * d) All of the above

**Answer:** d) All of the above

1. **Which tool in Cadence Allegro is primarily used to run a DRC?**
   * a) Constraint Manager
   * b) Layout Editor
   * c) DRC Check Tool
   * d) Schematic Editor

**Answer:** c) DRC Check Tool

1. **What kind of rule violations can DRC check for in a design?**
   * a) Trace width violations
   * b) Component clearance violations
   * c) Via size violations
   * d) All of the above

**Answer:** d) All of the above

1. **What happens when DRC detects a rule violation in the design?**
   * a) The system automatically fixes the error
   * b) A violation report is generated listing the errors
   * c) The design is saved and no further action is needed
   * d) The netlist is updated with the errors

**Answer:** b) A violation report is generated listing the errors

1. **In Cadence Allegro, which of the following is typically defined as a design rule for signal traces?**
   * a) Pin number
   * b) Trace width
   * c) Part number
   * d) Footprint size

**Answer:** b) Trace width

1. **Which of the following is NOT typically a check performed by DRC in Cadence Allegro?**
   * a) Component-to-component clearance
   * b) Pin-to-pin distance violations
   * c) Trace width and clearance violations
   * d) Verification of the functionality of the circuit

**Answer:** d) Verification of the functionality of the circuit

1. **Which Cadence Allegro tool is used to modify the constraints if a DRC violation occurs?**
   * a) Layout Editor
   * b) Constraint Manager
   * c) Netlist Generator
   * d) Schematic Editor

**Answer:** b) Constraint Manager

1. **What does the term “clearance” mean in the context of DRC?**
   * a) The space between components and traces
   * b) The size of the vias used in the design
   * c) The distance between power and ground nets
   * d) The pin number assignment for components

**Answer:** a) The space between components and traces

1. **Which of the following is true about running DRC in Cadence Allegro?**
   * a) DRC only checks the schematic, not the layout
   * b) DRC verifies that the design meets manufacturing constraints
   * c) DRC is run automatically whenever a design is saved
   * d) DRC is unnecessary if you are using simulation tools

**Answer:** b) DRC verifies that the design meets manufacturing constraints

1. **Which of the following is typically a DRC rule that applies to vias?**
   * a) Via pad size
   * b) Via hole size
   * c) Via-to-via clearance
   * d) All of the above

**Answer:** d) All of the above

1. **What is the result of ignoring or bypassing a DRC violation?**
   * a) The design may fail during manufacturing
   * b) The netlist will be automatically generated
   * c) The design will be automatically corrected
   * d) There will be no impact on the design

**Answer:** a) The design may fail during manufacturing

1. **What file format is typically used to export DRC results in Cadence Allegro?**
   * a) .log
   * b) .pdf
   * c) .drc
   * d) .txt

**Answer:** a) .log

1. **Which of the following can be specified as a DRC constraint in Cadence Allegro?**
   * a) Trace width
   * b) Component placement
   * c) Power distribution
   * d) Netlist generation

**Answer:** a) Trace width

1. **How can DRC violations be viewed in Cadence Allegro?**
   * a) Through the "Violation Summary" report
   * b) By opening the schematic file
   * c) By running a simulation
   * d) By checking the component properties

**Answer:** a) Through the "Violation Summary" report

1. **Which of the following actions should be taken if a DRC violation occurs?**
   * a) Fix the violation by adjusting the design or constraints
   * b) Ignore the violation if it doesn't affect functionality
   * c) Save the design and submit it for manufacturing
   * d) Revert to the previous design version

**Answer:** a) Fix the violation by adjusting the design or constraints

1. **Which of the following is NOT an example of a DRC violation that could be found in Cadence Allegro?**
   * a) Two traces are too close together
   * b) A pin is left unconnected
   * c) Component values are missing from the schematic
   * d) A via is too large for the design rule

**Answer:** c) Component values are missing from the schematic

1. **What should you do if you encounter a DRC violation that cannot be fixed easily?**
   * a) Skip the violation and continue with the design
   * b) Manually change the layout to correct the violation
   * c) Seek help from an experienced designer or refer to the design guidelines
   * d) Ignore it and proceed to generate the netlist

**Answer:** c) Seek help from an experienced designer or refer to the design guidelines